

REMARKS

Claims 1-8 and 19 are pending in the application. Claim 1 has been amended, and new claim 19 has been added by the present amendment. The amendment and added claim are fully supported by the application as originally filed (see, e.g., specification at page 5, lines 19-22; page 9, line 17 to page 10, line 16; page 12, lines 3-8; and FIGS. 4a-4c and 5).

As amended, independent claim 1 recites a multi-chip package device with a heat sink in which "a plurality of hollow parts extending through the heat sink are formed at a location of the heat sink subjected to **greatest thermal stresses**, and the plurality of hollow parts are formed **symmetrically** at an area of the heat sink free of contact with the first chip and the semiconductor package to release thermal stresses from the heat sink" (see, e.g., FIGS. 4a-4c and FIG. 5, and accompanying specification cited above; for example, the "greatest thermal stresses" language is described on page 5, lines 19-22 and page 12, lines 3-8; and the "symmetrically" language is described on page 9, line 24 to page 10, line 3).

Referring to FIGS. 4a-4c and 5, for example, a heat sink 34 is formed with at least one symmetrical pair of hollow parts 34a positioned at an area of the heat sink 34 free of contact with a first chip 32 and semiconductor packages 33 (see, e.g., page 9, line 24 to page 10, line 3 of the specification). As a result, thermal stresses of the heat sink 34 can be effectively released from locations of the heat sink subjected to the greatest stresses.

Claims 1-4 and 6-8 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent Application Publication US 2004/0099945 to Ku (hereinafter "Ku"). Claim 5 was rejected under 35 USC 103(a) as being unpatentable over Ku in view of U.S. Patent Application Publication US 2003/0089977 to Chee et al. These rejections are respectfully traversed.

Regarding the rejection of independent claim 1 over Ku, the Ku reference does not teach or suggest a multi-chip package device in which a plurality of hollow parts of a heat sink are formed **symmetrically** at an area of the heat sink free of contact with a first chip and a semiconductor package.

Referring to FIG. 4 and paragraphs 0048-0050 of Ku, a thermal bridge 50 is "buried" in an encapsulant 20, and the thermal bridge 50 includes apertures 504 which are not symmetrically positioned.

In Ku, since the apertures 504 are embedded in the encapsulant 20, the apertures 504 are not configured to relieve thermal stresses as claimed.

Further, referring to paragraph 0050 of Ku, the apertures 504 are provided "to accommodate the chips for saving material and facilitating the flow path design in forming the encapsulant 20 on the substrate 10," where the apertures 504 have a location and size restricted by the arrangement of chips 30, 31, and thus would not be capable of releasing thermal stresses from locations subject to the greatest thermal stresses.

On page 3 of the Office Action of 05/23/2008 (and repeated in the "Response to Arguments" section on page 6 of the Office Action), the encapsulant 20 of Ku was cited as allegedly corresponding to the Applicant's claimed "semiconductor package."

However, one of ordinary skill in the art would understand that an *encapsulant*, such as the encapsulant 20 of Ku "for covering and sealing the chips 30, 31 on the substrate 10" (paragraph 0048 of Ku) does not correspond to the Applicant's claimed "semiconductor package."

Moreover, even if the encapsulant 20 of Ku is somehow considered a "semiconductor package," since the thermal bridge 50 is "buried" in the encapsulant 20 (paragraph 0048 of Ku), and thus the apertures 504 of the thermal bridge 50 are embedded in the encapsulant 20 (paragraph 0050 of Ku), there is no teaching or suggestion in Ku of the Applicant's claimed plurality of hollow parts that are formed "at an area free of contact with the first chip and the semiconductor package" (see independent claim 1, emphasis added).

For at least the reasons discussed above, the Ku reference does not anticipate or otherwise render obvious the Applicant's claimed invention. Therefore, independent claim 1 and dependent claims 2-8 and 19 are patentable over Ku.

Further, regarding the rejection of claim 6, as shown in FIGS. 4 and 10 of Ku, it is clear that the chips 30 and 31 are not mounted at a center of the substrate 10, and the encapsulant 20 is not mounted at a position on the substrate 10 corresponding to a corner of the thermal bridge 50.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

/Steven M. Jensen/

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Steven M. Jensen
(Reg. No. 42,693)
Edwards Angell Palmer & Dodge
P.O. Box 55874
Boston, MA 02205

Phone: (617) 239-0100

Customer No. 21874